

Deliverable 2.2

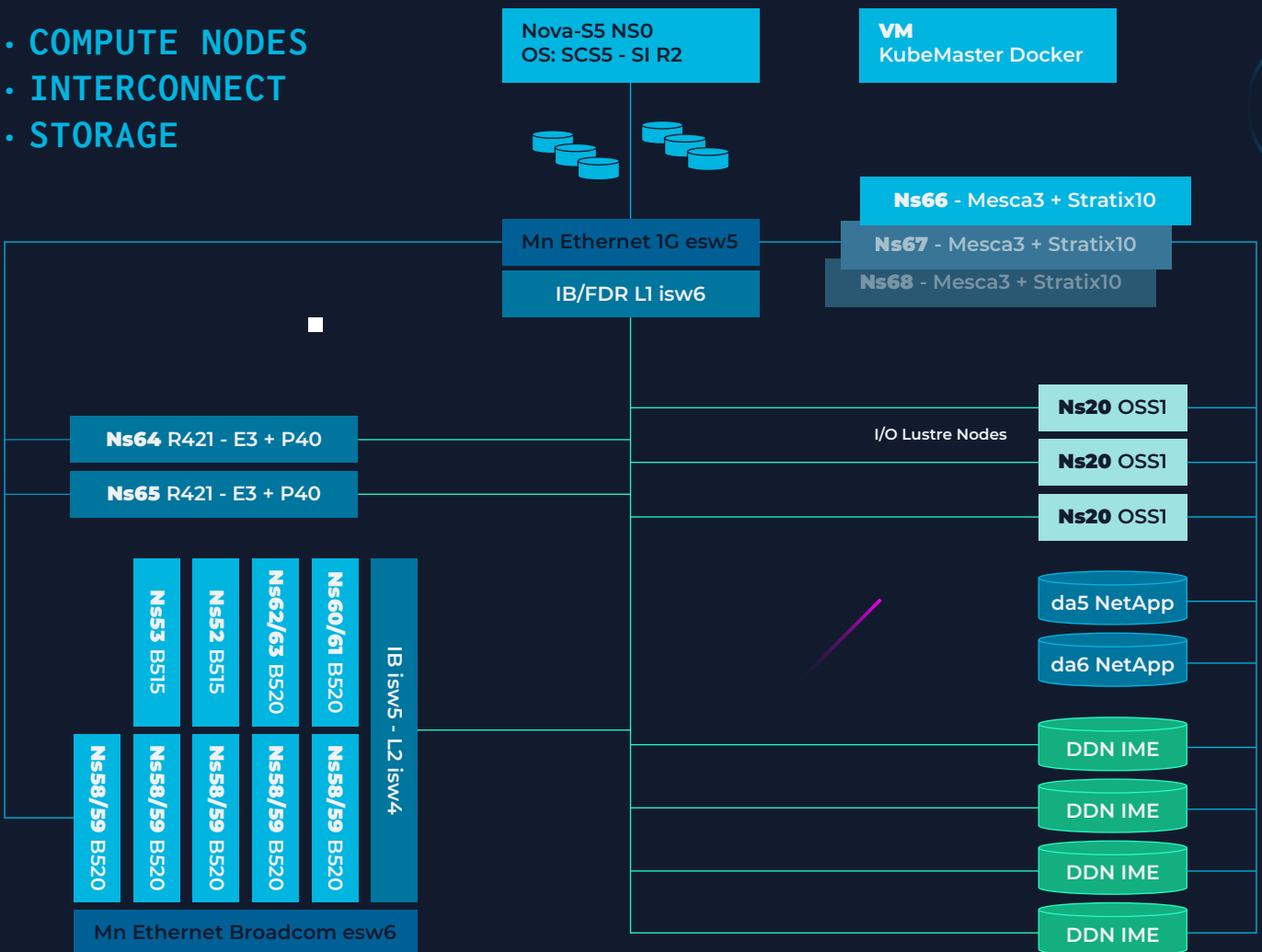
Description and access to converged hardware platform

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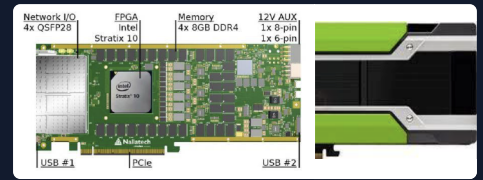
GOALS OF THE DELIVERABLE

- Define strategy to control the release of system software components

- COMPUTE NODES
- INTERCONNECT
- STORAGE

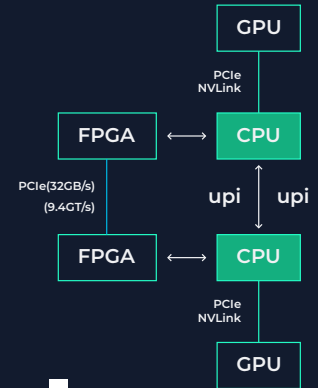
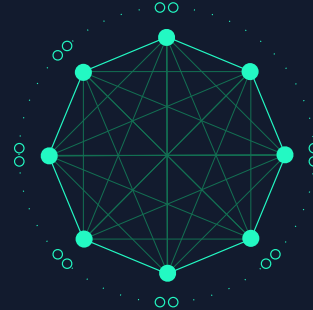


ACCELERATED COMPUTING



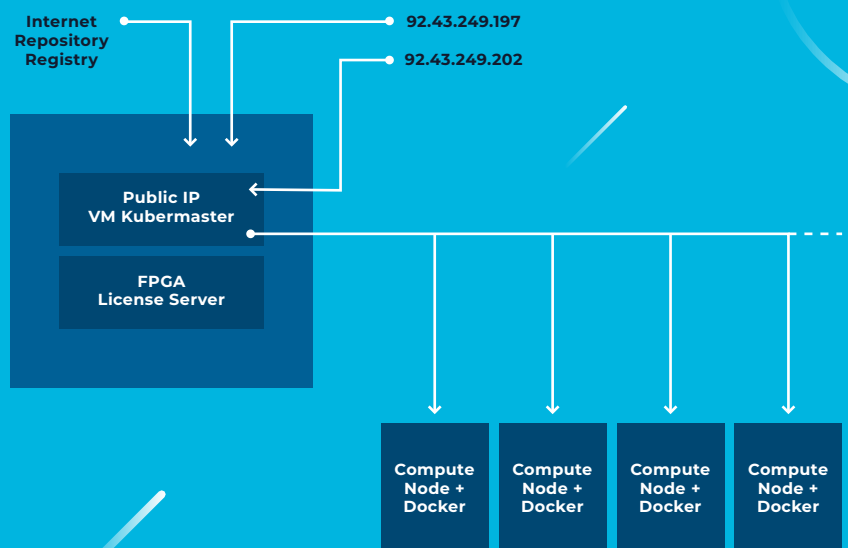
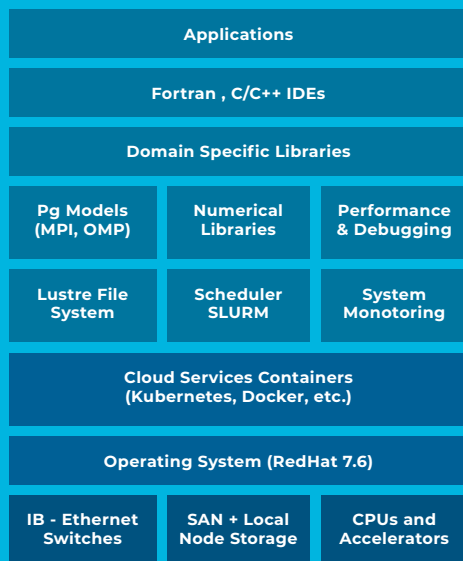
- Discrete Integration of compute Node
- Acceleration Technologies

- Nvidia/P40: 3840 Cores, 24GB GDDR5, PCIe 3.0
- GPU/V100: 5120 Cores, 32GB HBM2, Pcie Gen3
- Nallatech/520N
 - Intel/Stratix 10 GX 2800
 - 4x QSFP28s for 400Gbps
 - BittWare-optimized OpenCL BSP
- Programming Models CUDA, OpenCL, RTL



DESCRIPTION AND ACCESS TO CONVERGED HARDWARE PLATFORM

- HPC SOFTWARE STACK
- DOCKER CONTAINER
- KUBERNETES ORCHESTRATOR



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